
**MOTOROLA**
# SEMICONDUCTOR
**TECHNICAL DATA**
# MPC555
Product Preview
# PowerPC ™ Microcontroller

**Features**

•PowerPC ™ Core with Floating-Point Unit
•26 Kbytes Fast RAM and 6 Kbytes TPU Microcode RAM
•448 Kbytes Flash EEPROM with 5V Programming
•5V I/O System
•Serial System: Queued Serial Multi-Channel Module (QSMCM), Dual CAN 2.0B Controller Modules (TouCAN ™ )
•50-Channel Timer System: Dual Time Processor Units (TPU3), Modular I/O System (MIOS1)
•32 Analog Inputs: Dual Queued Analog-to-Digital Converters (QADC64)
•Submicron HCMOS (CDR1) Technology
•272-Pin Plastic Ball Grid Array (PBGA) Packaging
•40-MHz operation, -40° C to 125° C with Dual Supply (3.3V, 5V)

**RISC MCU Central Processing Unit (RCPU)**

•32-Bit PowerPC ™ Architecture (compliant with PowerPC ™ Architecture Book 1)
•Core performance measured at 52.7K Dhrystones (v2.1) @ 40 MHz
•Fully static, low power operation
•Integrated double-precision floating-point unit
•Precise exception model
•Extensive system development support
-On-chip watchpoints and breakpoints
-Program flow tracking
-BDM on-chip emulation development interface

**Four-Bank Memory Controller**

•Works with SRAM, EPROM, flash EEPROM, and other peripherals
•Byte write enables
•32-bit address decodes with bit masks

**U-Bus System Interface Unit (USIU)**

•Clock synthesizer
•Power management
•Reset controller
•PowerPC ™ decrementer and time base
•Real-time clock register
•Periodic interrupt timer
•Hardware bus monitor and software watchdog timer
•Interrupt controller that supports up to eight external and eight internal interrupts
•IEEE 1149.1 JTAG test access port
•External bus interface
-24 address pins, 32 data pins
-Supports multiple master designs
-Four-beat transfer bursts, two-clock minimum bus transactions
-Supports 5V inputs, provides 3.3V outputs

**Flexible Memory Protection Unit**

•Four instruction regions and four data regions
•4-Kbyte to 16-Mbyte region size support
•Default attributes available in one global entry
•Attribute support for speculative accesses

**448-Kbyte Flash EEPROM Memory**

•One 256-Kbyte and one 192-Kbyte module
•Page read mode
•Block (32-Kbyte) erasable
•External 4.75V to 5.25V program and erase power supply

**26-Kbytes of Static RAM**

•One 16-Kbyte and one 10-Kbyte module
•Fast (one-clock) access
•Keep-alive power
•Soft defect detection (SDD)

**General-Purpose I/O Support**

•Address (24) and data (32) pins can be used for general-purpose I/O in single-chip mode
•9 general-purpose I/O pins in MIOS1 unit
•Many peripheral pins can be used for general-purpose I/O when not used for primary function
•5V tolerant inputs/outputs

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**Queued Serial Multi-Channel Module (QSMCM)**

•Queued serial peripheral interface (QSPI)
-Provides full-duplex communication port for peripheral expansion or interprocessor communi-cation
-Up to 32 preprogrammed transfers, reducing overhead
-160-byte queue buffer
-Programmable transfer length: from 8 to 16 bits, inclusive
-Synchronous interface with baud rate of up to system clock divided by 4
-Four programmable peripheral-select pins support up to 16 devices
-Wrap-around mode allows continuous sampling for efficient interfacing to serial peripherals (e.g. serial A/D converters, I/O latches, etc.)
•Two serial communications interfaces (SCI). Each SCI offers these features:
-UART mode provides NRZ format and half-or full-duplex interface
-16 register receive buffer and 16 register transmit buffer (SCI1 only)
-Advanced error detection and optional parity generation and detection
-Word length programmable as 8 or 9 bits
-Separate transmitter and receiver enable bits and double buffering of data
-Wakeup functions allow the CPU to run uninterrupted until either a true idle line is detected or a new address byte is received
-External source clock for baud generation
-Multiplexing of transmit data pins with discrete outputs and receive data pins with discrete in-puts, allowing realization of a low-speed serial protocol